ANALOG DEVICES

Low-Power Precision Operational Amplifier

PM-1012

FEATURES

- **Low Supply Current** ..... **600μA Max**
- **Very Low Offset** ..... **35μV Max**
- **Low Drift** ..... **1.5μV/°C Max**
- **Very Low Bias Current**
  - **25°C** ..... **100pA Max**
  - **−55°C to +125°C** ..... **250pA Max**
- **Low Noise** ..... **0.5μV_{p-p} Typ**
- **High Common-Mode Rejection** ..... **114dB Min**
- **Available In Die Form**

ORDERING INFORMATION †

V_{OS} (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
35	PM1012AJ*	PM1012AZ*	–	MIL
50	PM1012GJ	PM1012GZ	–	COM
50	–	–	PM1012GP	XIND
50	–	–	PM1012GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

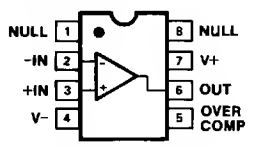
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PM-1012 is a general-purpose, precision operational amplifier. Offering several performance enhancements over industry-standard precision op amps such as the OP-07, the PM-1012 requires less than 1/6 the supply current. These enhancements include exceptionally low bias currents of only ±80pA, typical, over the full military temperature range and 132dB of common-mode rejection and power-supply rejection. The PM-1012's low offset voltage of 35μV maximum frees the user from external nulling in most circuits.

An open-loop gain of two million into a 10kΩ load ensures that excellent linearity is maintained even in high-gain configurations, and 5mA of output current allows 2kΩ loads to be driven

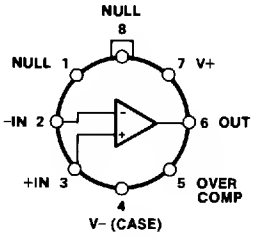
PIN CONNECTIONS



EPOXY MINI-DIP
(P-Suffix)

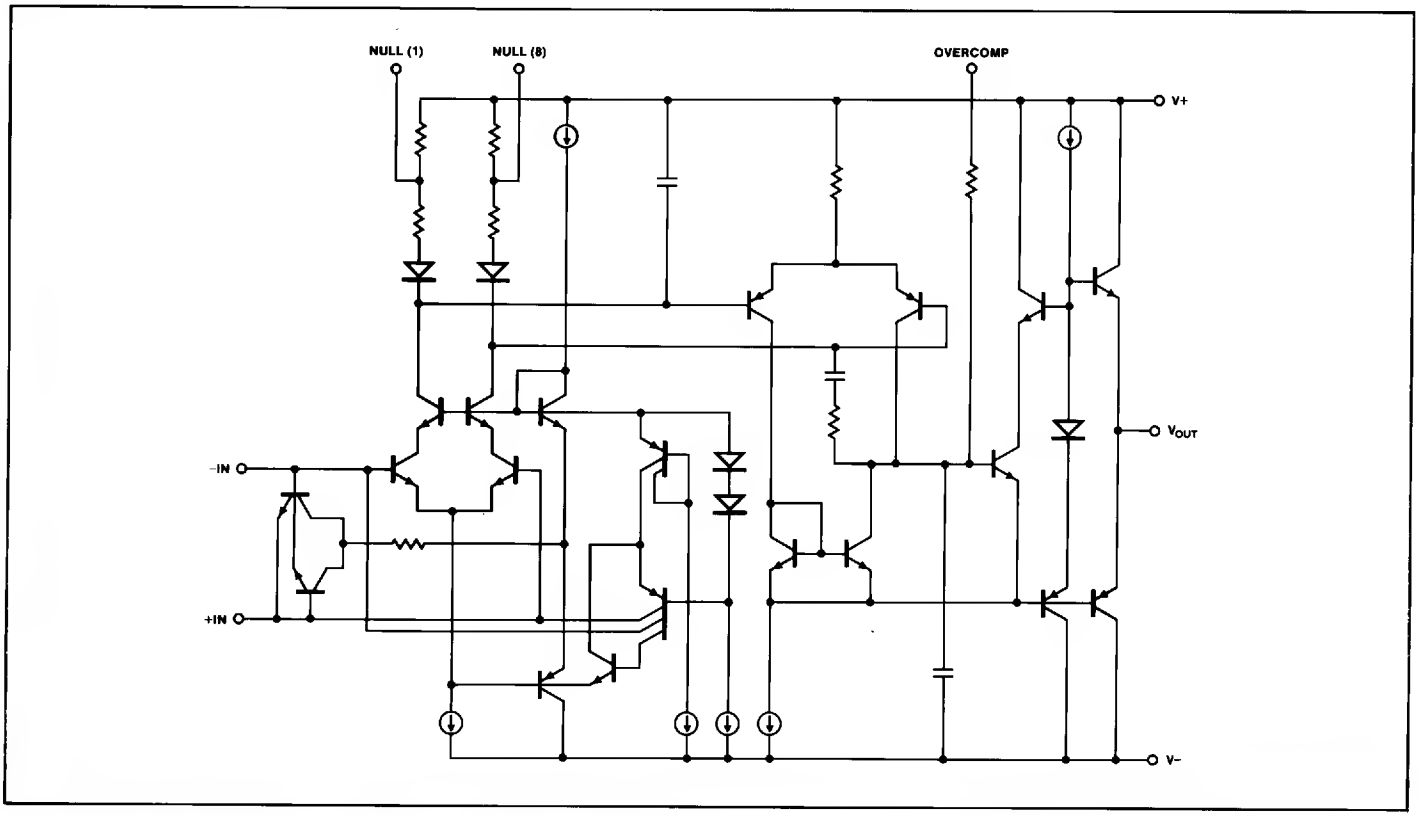
8-PIN HERMETIC DIP
(Z-Suffix)

EPOXY SO
(S-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



with an open-loop gain of one million. The PM-1012 offers low noise, especially for a low-power amplifier — only 17nV/$\sqrt{Hz}$ at 10Hz. Exceptionally low current-noise minimizes noise contributions when high source impedances are used. The PM-1012 may be overcompensated using pin 5 to limit the amplifier's bandwidth, further reducing system noise and increasing stability with large capacitive loads.

The PM-1012 conforms to the OP-07 pinout with nulling through pins 1 and 8 to the positive supply. It offers an upgrade to the OP-07 in sockets where reduced power dissipation or low bias currents are attractive. It may also be used as an upgrade from the OP-12, OP-05 and 725 type op amps. The PM-1012 may replace 741 type op amps by removing the nulling potentiometer, if used. For an externally compensated amplifier sharing many of the PM-1012's precision specifications, see the PM-1008 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... **±20V**
Input Voltage (Note 3) ..... **±20V**
Differential Input Voltage (Note 4) ..... **±1V**
Differential Input Current (Note 4) ..... **±10mA**
Output Short-Circuit Duration ..... **Indefinite**

Operating Temperature Range
PM-1012A (J,Z) ..... –55°C to +125°C
PM-1012G (J,Z) ..... 0°C to +70°C
PM-1012G (P,S) ..... –40°C to +85°C
Storage Temperature Range ..... –65° to +150°C
Junction Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{jA} (Note 2)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.
3. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
4. The PM-1012's inputs are protected by back-to-back diodes. Current- limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted.

			PM-1012A			PM-1012G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	8	35	—	10	50	µV
		(Note 1)	—	20	90	—	25	120	
Long-Term V_{OS} Stability	ΔV_{OS}/Time		—	0.3	—	—	0.3	—	µV/month
Input Offset Current	I_{OS}		—	15	100	—	20	150	pA
		(Note 1)	—	25	150	—	30	200	
Input Bias Current	I_B		—	±25	±100	—	±30	±150	pA
		(Note 1)	—	±35	±150	—	±40	±200	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	17	30	—	17	30	nV/$\sqrt{Hz}$
		f_O = 1000Hz (Note 4)	—	14	22	—	14	22	
Input Noise Current Density	i_N	f_O = 10Hz	—	20	—	—	20	—	fA/$\sqrt{Hz}$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12V$; $R_L = 10k\Omega$	300	2000	—	200	2000	—	V/mV
		$V_O = \pm 10V$; $R_L = 2k\Omega$	200	1000	—	120	1000	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	114	132	—	110	132	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	114	132	—	110	132	—	dB
Input Voltage Range	IVR	(Note 2)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.1	0.2	—	0.1	0.2	—	V/µs
Full-Power Bandwidth	BW_P		—	3	—	—	3	—	kHz
Gain-Bandwidth Product	GBW	$A_V = 100$	—	0.5	—	—	0.5	—	MHz
Supply Current	I_{SY}	(Note 1)	—	380	600	—	380	600	µA
Supply Voltage	V_S	Operating Range	±2	±15	±20	±2	±15	±20	V

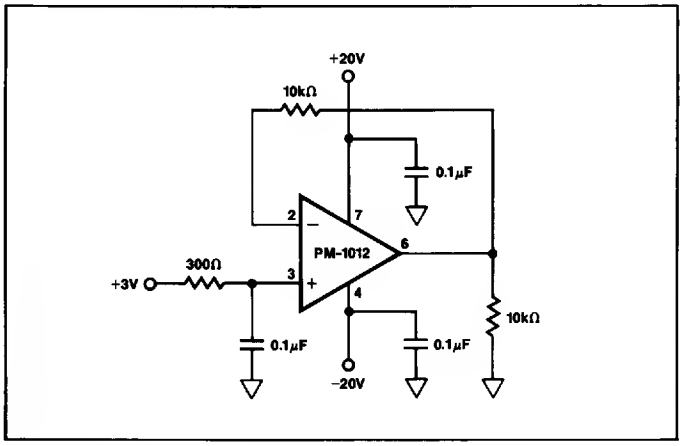
NOTES:
1. These specifications apply for $\pm 2V \le V_S \le \pm 20V$ and $-13.5V \le V_{CM} \le +13.5V$ (for $V_S = \pm 15V$).
2. Guaranteed by CMR test.
3. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
4. Sample Tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq +70°C$ for PM-1012 GJ and GZ, $-40°C \leq T_A \leq +85°C$ for PM1012GP, GS and $-55°C \leq T_A \leq +125°C$ for PM-1012A, unless otherwise noted.

			PM-1012A			PM-1012G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	30	180	—	20	120	μV
		(Note 1)	—	40	250	—	30	200	
Average Temperature Coefficient of V_{OS}	TCV_{OS}		—	0.2	1.5	—	0.2	1.5	μV/°C
Input Offset Current	I_{OS}		—	30	250	—	20	230	pA
		(Note 1)	—	70	350	—	40	300	
Average Temperature Coefficient of I_{OS}	TCI_{OS}		—	0.3	2.5	—	0.3	2.5	pA/°C
Input Bias Current	I_B		—	±50	±250	—	±35	±230	pA
		(Note 1)	—	±80	±350	—	±50	±300	
Average Temperature Coefficient of I_B	TCI_B		—	0.3	2.5	—	0.3	2.5	pA/°C
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12V$; $R_L = 10k\Omega$	150	1000	—	150	1500	—	V/mV
		$V_O = \pm 10V$; $R_L = 2k\Omega$	100	600	—	100	800	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	108	128	—	108	130	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2.5V$ to $\pm 20V$	108	126	—	108	128	—	dB
Input Voltage Range	IVR	(Note 2)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.05	0.15	—	0.05	0.15	—	V/μs
Supply Current	I_{SY}	(Note 1)	—	400	800	—	400	800	μA
Supply Voltage	V_S	Operating Range	±2.5	±15	±20	±2.5	±15	±20	V

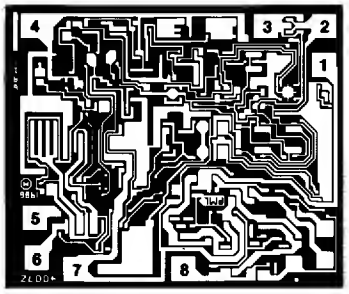
NOTES:
1. These specifications apply for $\pm 2.5V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
2. Guaranteed by CMR test.

BURN-IN CIRCUIT



PM-1012

DICE CHARACTERISTICS



DIE SIZE 0.063 × 0.074 inch, 4662 sq. mils
(1.60 × 1.88 mm, 3.01 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
5. OVERCOMPENSATION
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-1012N LIMIT	UNITS
Input Offsat Voltaga	V_{OS}	(Nota 1) (Note 2)	250 300	μV MAX
Input Offsat Currant	I_{OS}	(Note 2)	150 200	pA MAX
Input Bias Current	I_B	(Note 2)	±150 ±200	pA MAX
Larga-Signal Voltage Gain	A_{VO}	$V_{OUT} = \pm 12V$, $R_L = 10k\Omega$ $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$	200 120	V/mV MIN
Common-Moda Rejection	CMR	$V_{CM} = \pm 13.5V$	110	dB MIN
Powar-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	110	dB MIN
Input Voltaga Range	IVR	(Note 3)	±13.5	V MIN
Output Voltaga Swing	V_O	$R_L = 10k\Omega$	±13	V MIN
Slaw Rata	SR		0.1	V/μs MIN
Supply Currant	I_{SY}	No Load	600	μA MAX

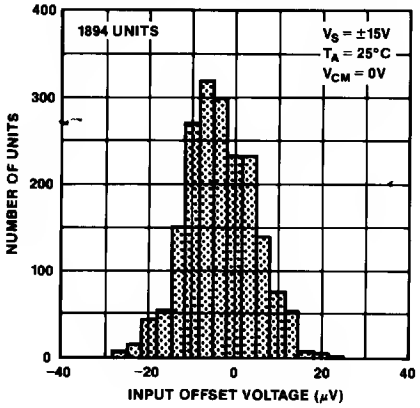
NOTES:

1. Final offset trims are not parformed on dice. These trims are typically performed after packaging. Precision Monolithics Inc. assumes no rasponsibility for impropar trimming by tha customer. Contact factory for trim methods.
2. Thesa specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
3. Guaranteed by CMR tast.

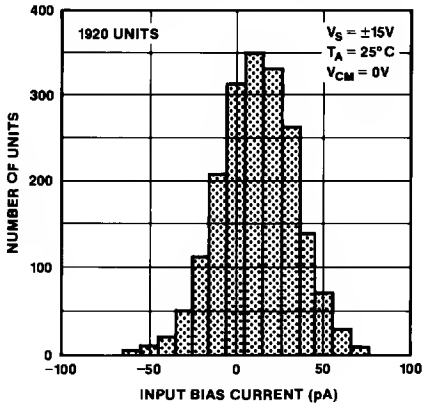
Electrical tasts ara parformad at wafer probe to the limits shown. Due to variations in assambly methods and normal yield loss, yiald after packaging is not guaranteed for standard product dice. Consult factory to nagotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

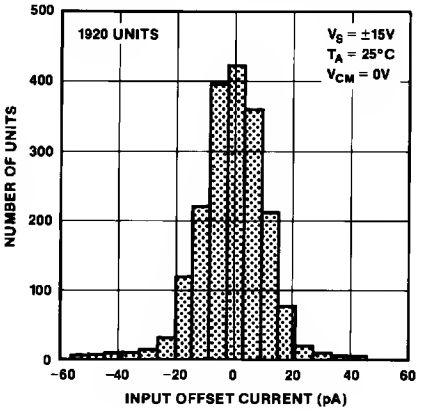
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



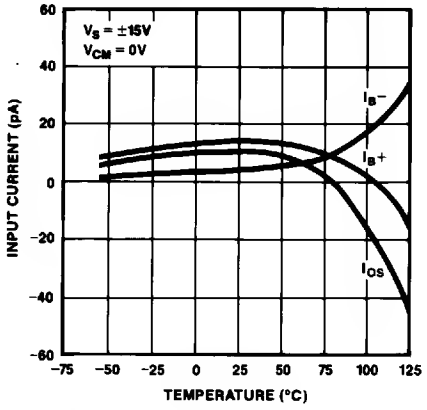
TYPICAL DISTRIBUTION OF INPUT BIAS CURRENT



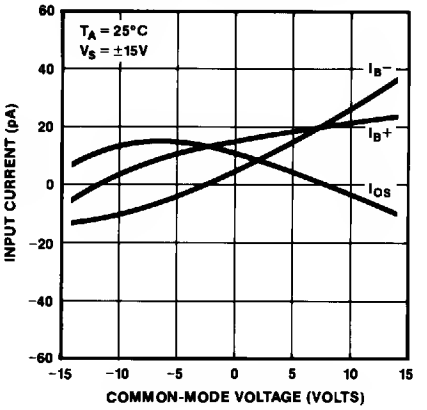
TYPICAL DISTRIBUTION OF INPUT OFFSET CURRENT



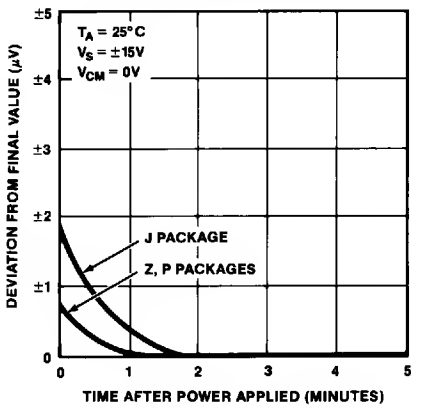
INPUT BIAS, OFFSET CURRENT vs TEMPERATURE



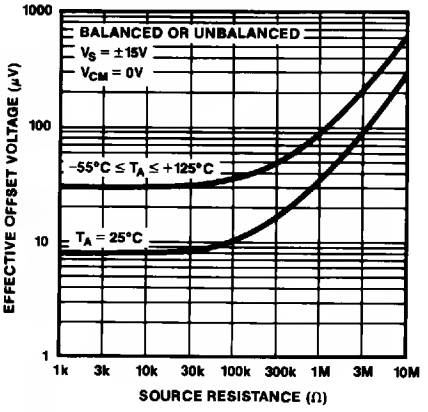
INPUT BIAS, OFFSET CURRENT vs COMMON-MODE VOLTAGE



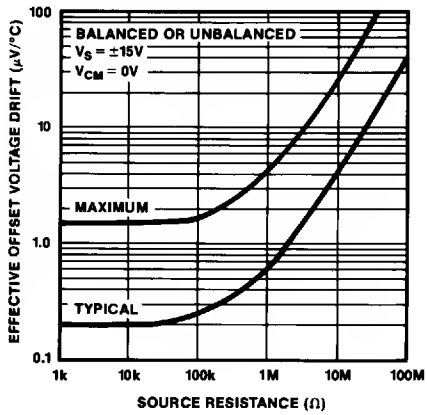
INPUT OFFSET VOLTAGE WARM-UP DRIFT



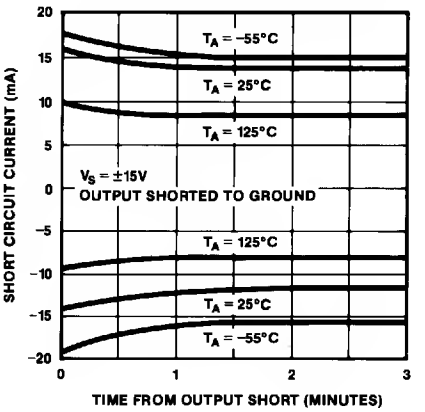
EFFECTIVE OFFSET VOLTAGE vs SOURCE RESISTANCE



EFFECTIVE TCV_{OS} vs SOURCE RESISTANCE

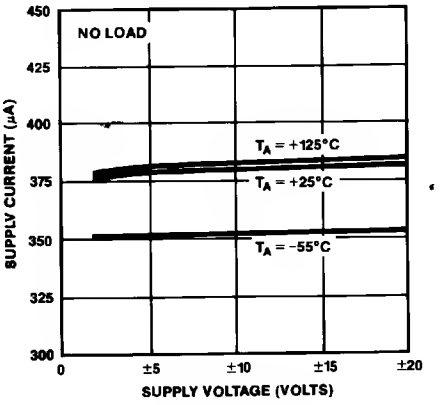


SHORT CIRCUIT CURRENT vs TIME, TEMPERATURE

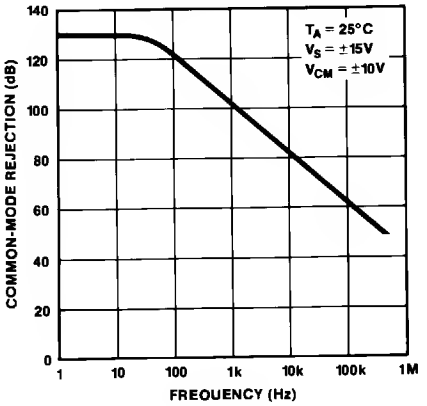


TYPICAL PERFORMANCE CHARACTERISTICS

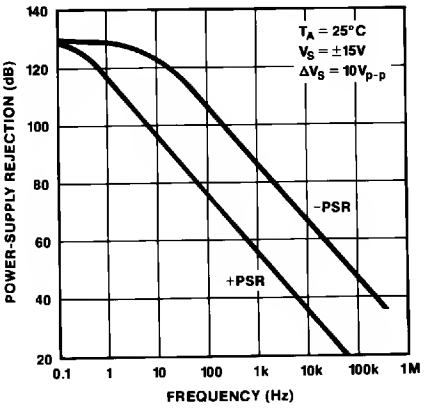
SUPPLY CURRENT vs SUPPLY VOLTAGE



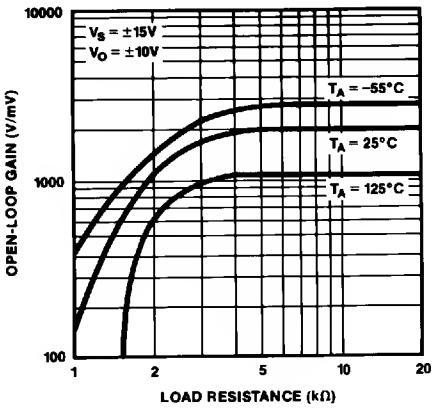
COMMON-MODE REJECTION vs FREQUENCY



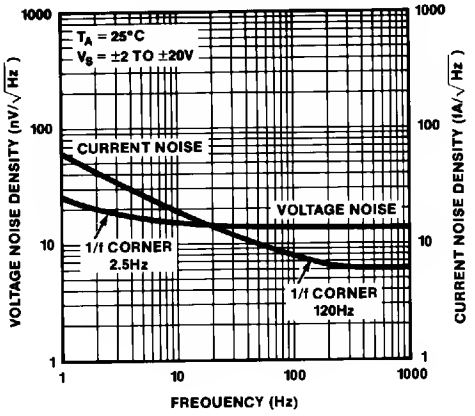
POWER-SUPPLY REJECTION vs FREQUENCY



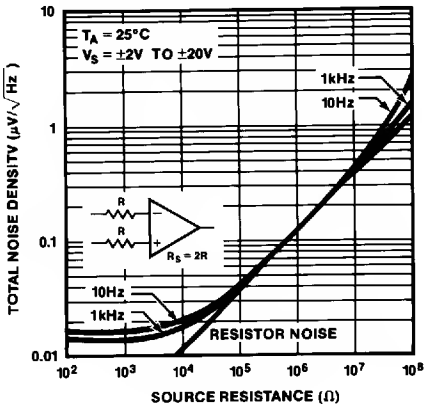
OPEN-LOOP GAIN vs LOAD RESISTANCE



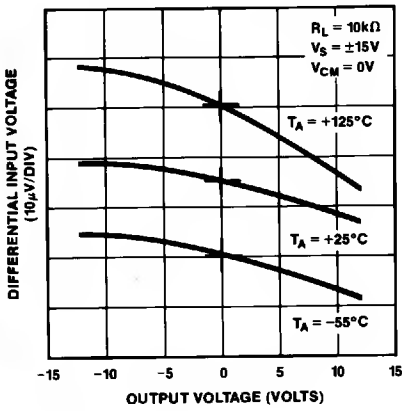
NOISE DENSITY vs FREQUENCY



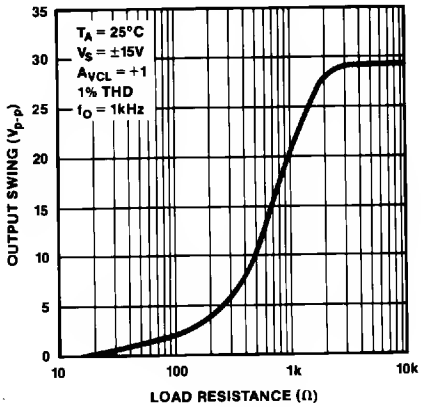
TOTAL NOISE DENSITY vs SOURCE RESISTANCE



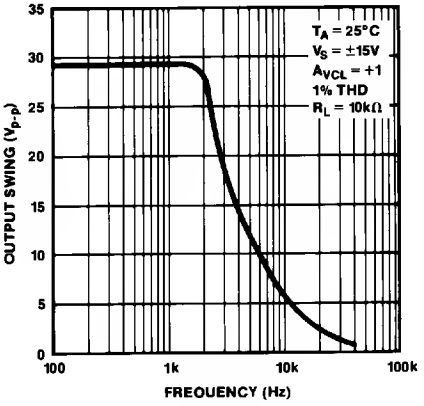
OPEN-LOOP GAIN LINEARITY



MAXIMUM OUTPUT SWING vs LOAD RESISTANCE

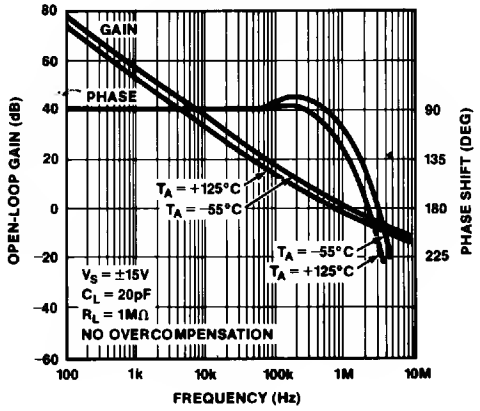


MAXIMUM OUTPUT SWING vs FREQUENCY

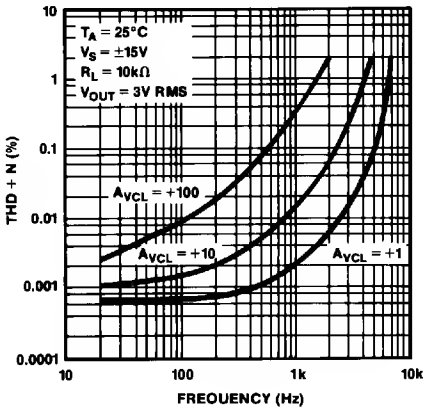


TYPICAL PERFORMANCE CHARACTERISTICS

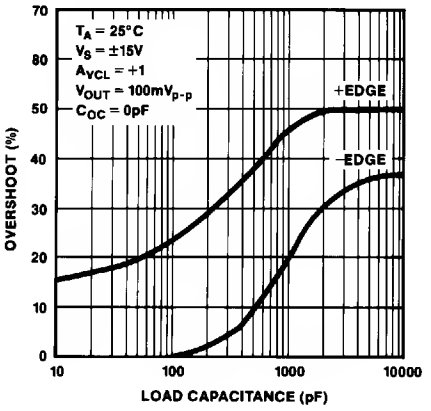
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 0pF)



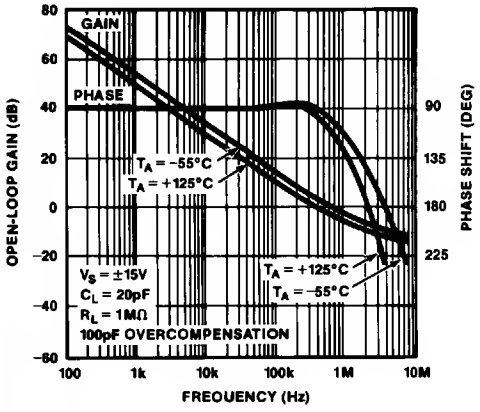
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



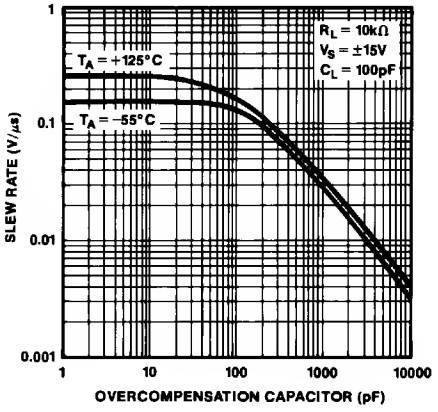
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



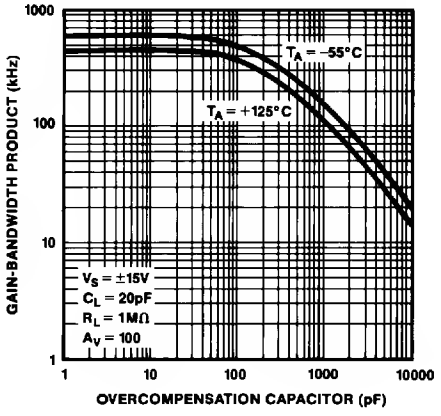
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 100pF)



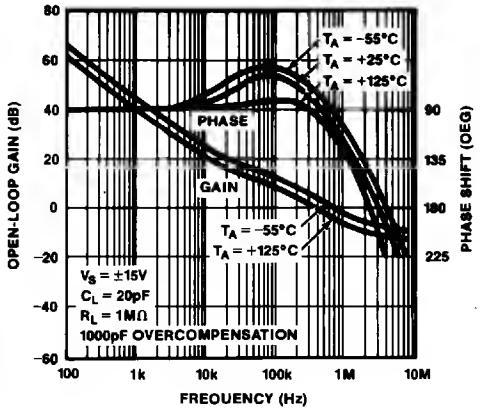
SLEW RATE vs OVERCOMPENSATION



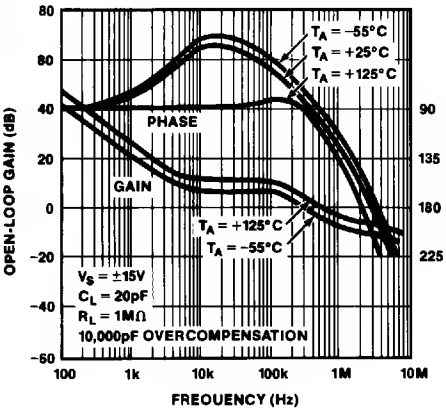
GAIN-BANDWIDTH PRODUCT vs OVERCOMPENSATION



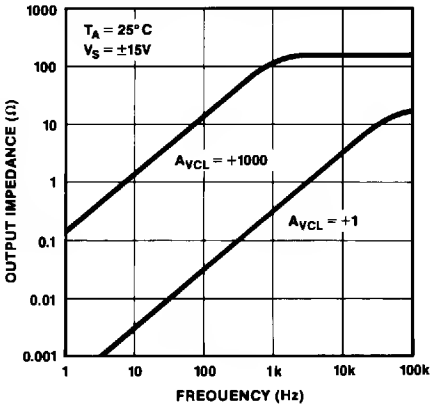
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 1000pF)



OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 10,000pF)



CLOSED-LOOP OUTPUT RESISTANCE vs FREQUENCY



APPLICATIONS INFORMATION

The PM-1012 is an ideal amplifier for general-purpose applications where precision is critical and power dissipation must be minimized. Excellent input specifications and a wide supply-voltage range allows the PM-1012 to be stocked as a standard amplifier for a wide variety of circuits. Overall performance of the PM-1012 is similar to, and in many respects better than traditional amplifiers such as the OP-07, and the PM-1012 will directly upgrade these sockets.

Extremely low bias current over the full military temperature range makes the PM-1012 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the PM-1012. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the PM-1012 are protected against large differential voltages by back-to-back diodes. Current-limiting resistors are not used so that low-noise performance is maintained. If differential voltages above ±1V are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10mA. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The PM-1012 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as ±2V. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10kΩ load.

Offset nulling is achieved utilizing the same circuitry as an OP-07. A potentiometer between 5kΩ and 100kΩ is connected between pins 1 and 8 with the wiper connected to the positive supply. The trim range is between 300μV and 850μV, depending upon the internal trimming of the device.

FIGURE 1: Optional Input Offset Voltage Nulling and Overcompensation Circuits

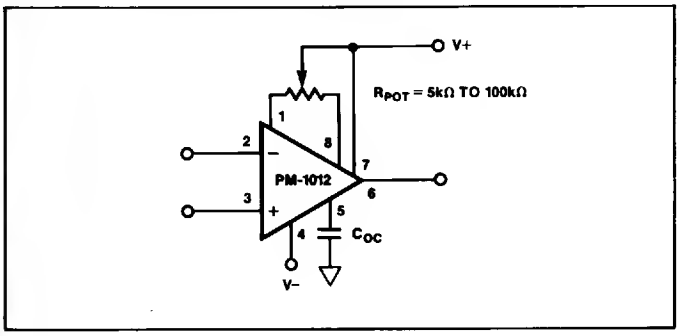
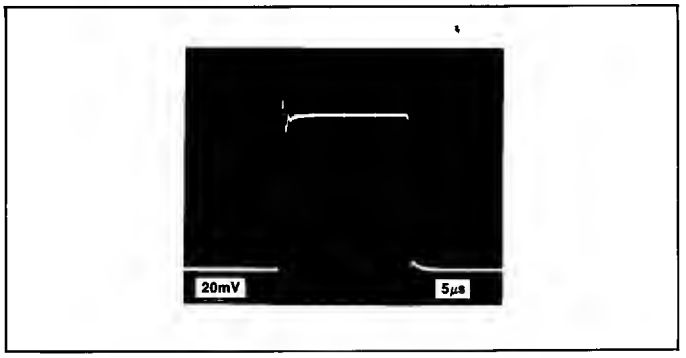


FIGURE 2: Small Signal Transient Response (C_{LOAD} = 100pF, A_{VCL} = +1)



AC PERFORMANCE

The PM-1012's AC characteristics are highly stable over its full operating temperature range. Unity-gain small signal response is shown in Figure 2. Extremely tolerant of capacitive loading on the output, the PM-1012 displays excellent response even with 1000pF loads (Figure 3). In large-signal applications, the input protection diodes effectively short the input to the output during the transients if the amplifier is connected in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved large-signal transient response is obtained by using a feedback resistor between the output and the inverting input. Figure 4 shows the large-signal response of the PM-1012 in unity-gain with a 10kΩ feedback resistor. The unity-gain follower circuit is shown in Figure 5.

FIGURE 3: Small-Signal Transient Response (C_{LOAD} = 1000pF, A_{VCL} = +1)

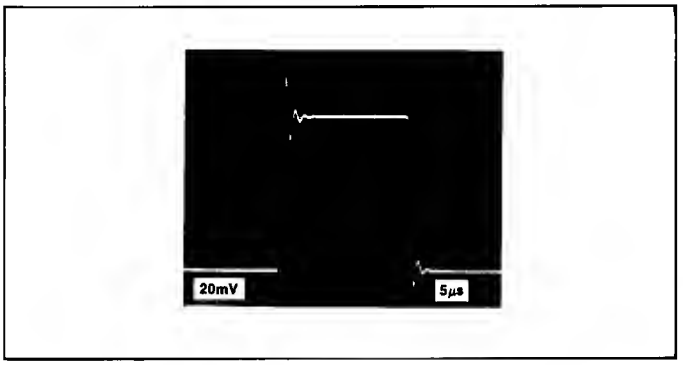


FIGURE 4: Large Signal Transient Response ($A_{VCL} = +1$)

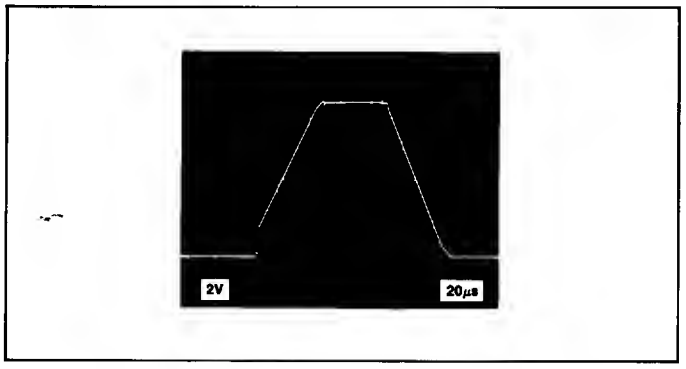
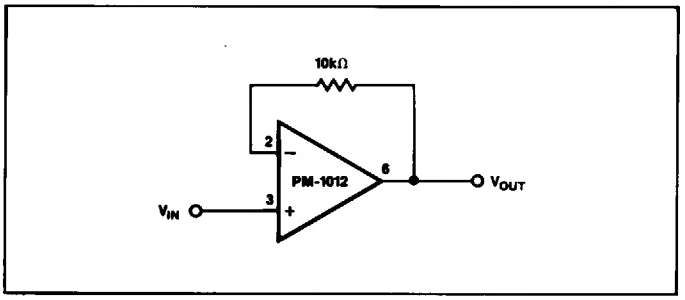


FIGURE 5: Unity-Gain Follower



USING OVERCOMPENSATION

The overcompensation pin provides flexibility for shaping AC response to an application's requirements. This pin may be used to increase the stability of circuits with large capacitive loads or gain in the feedback loop, or for feedforward compensation to improve slew rate.

Figure 6 shows feedforward compensation for a unity-gain follower. Slew rate is increased to close to 10V/µs in this circuit. Load driving ability is adversely affected by this compensation, and gain errors are incurred even with 10kΩ loads. Feedforward compensation should be used with care to ensure that significant errors are not introduced.

Capacitive load driving ability is improved by using overcompensation in the circuit of Figure 1. The signal response in Figure 8 was made under the same conditions as Figure 3, except for the addition of a 220pF capacitor placed between pin 5 and ground. Overcompensation in this manner increases phase margin and decreases the gain-bandwidth product of the amplifier.

FIGURE 6: Follower Feedforward Compensation

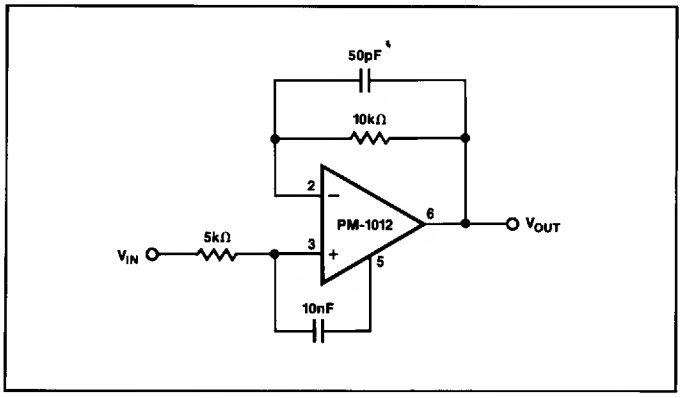


FIGURE 7: Feedforward Compensation Transient Response

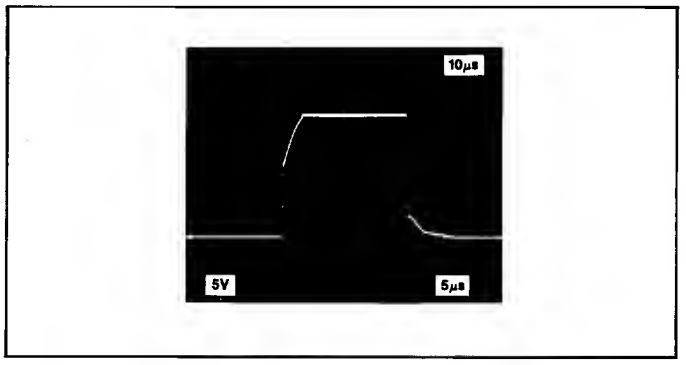
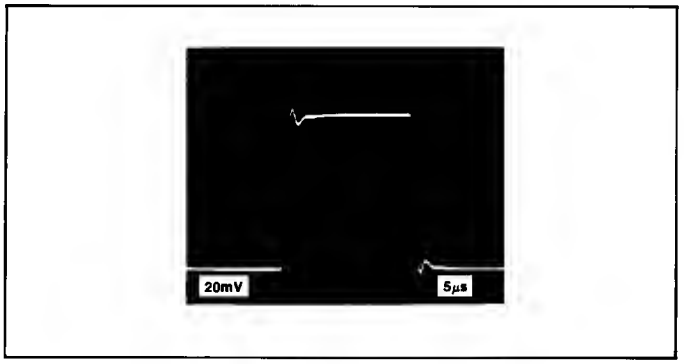


FIGURE 8: Small Signal Transient Response with Overcompensation (C_{LOAD} = 1000pF, $A_{VCL} = +1$, C_{OC} = 220pF)



GUARDING AND SHIELDING

To maintain the extremely high input impedances of the PM-1012, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces, so that guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Guard traces should be made on both sides of the circuit board.

High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

A precision absolute-value current-to-voltage converter that operates over a wide temperature range is shown in Figure 10. The PM-1012's low bias current over its full common-mode and temperature ranges ensures a high degree of linearity in this circuit. The PM-1012 acts as an inverting or noninverting current-to-voltage converter, depending upon the polarity of the input. While the input is sinking current, the voltage is developed across the resistor at the noninverting input, hence sources must have reasonable compliance. While the input is sourcing current, it remains at one diode drop below ground; compliance of a current sink at the input is less critical. If 1MΩ resistors are used, the circuit will output 1V/μA of input current.

FIGURE 9: Guard Ring Layout and Connections

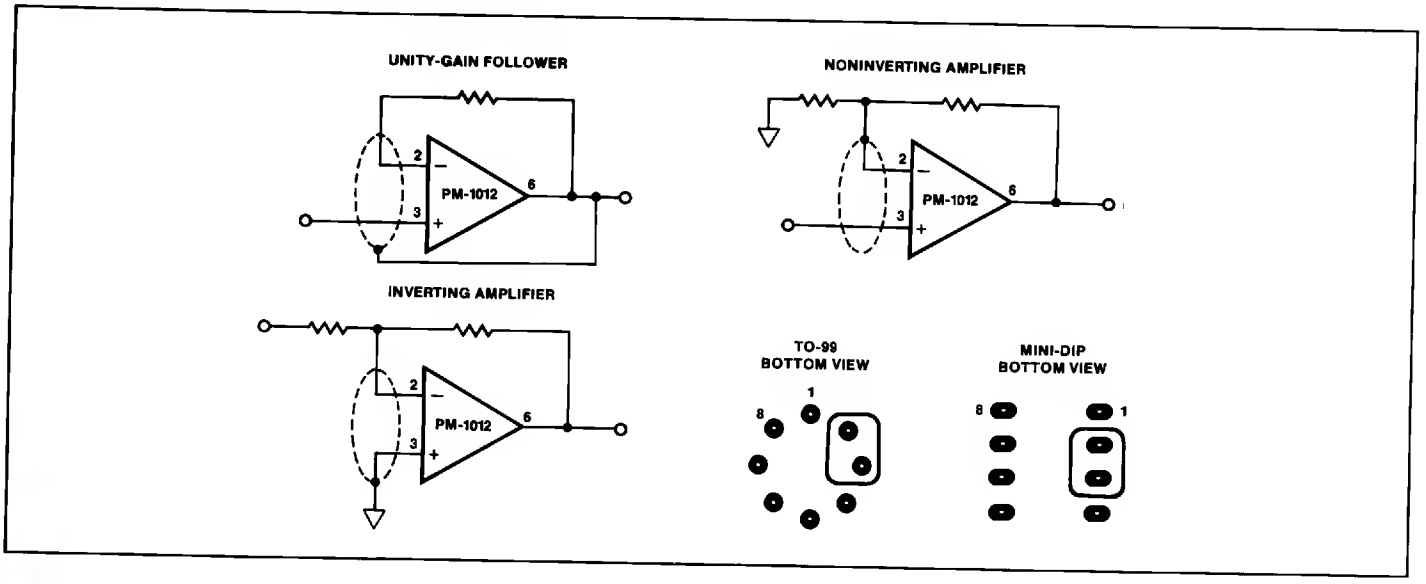


FIGURE 10: Precision Absolute-Value Current-to-Voltage Converter

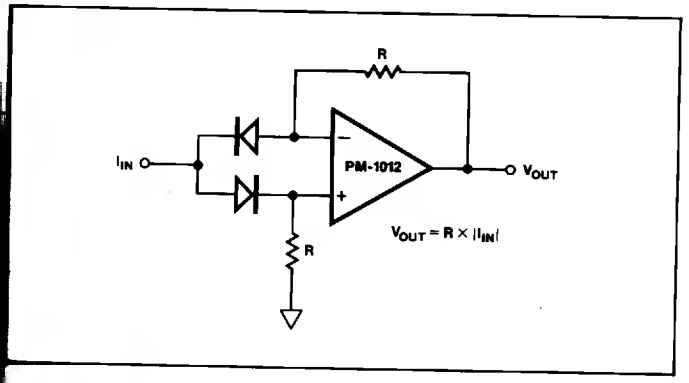
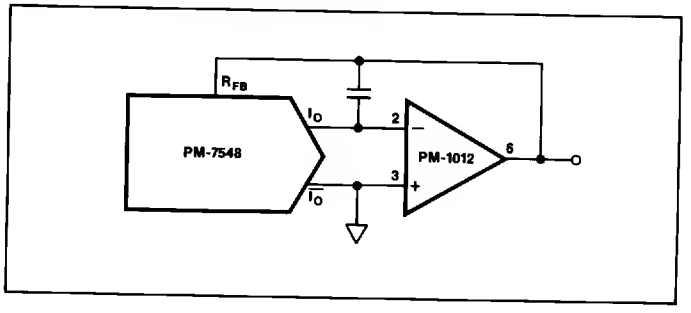


FIGURE 11: DAC Output Amplifier



The PM-1012 is an excellent amplifier for CMOS and bipolar DACs where high linearity is critical. Its low bias current and offset voltage ensures that linearity errors are negligible, even when operating with high resolution DACs and low reference voltages. A capacitor should be placed in the feedback loop of the amplifier to cancel the pole formed by the additional input capacitance from the DAC. Twenty to forty picofarads is usually adequate for compensation with CMOS or bipolar DACs.

The logarithmic amplifier in Figure 12 eliminates thermal drift caused by temperature dependencies of the logging transistors by maintaining a monolithic quad matched transistor at a predetermined temperature. The MAT-04 has four transistors laid-out at the corners of a square die. Two transistors across a diagonal are used for logging elements. One of the remaining transistors is used as a heater to maintain a constant chip temperature, and the remaining transistor, diagonally opposite to the heater, is used as a temperature sensor.

The OP-90 servo amplifier uses thermal feedback to set the temperature of the die. The base-to-emitter voltage of Q2 is maintained at the level set by the resistive divider from the REF-01, by controlling the current flowing through Q4. Although Q4 may operate at higher than the MAT-04's rated levels, this does not degrade operation since the characteristics of the heater transistor are non-critical. For best thermal regulation, the MAT-04 package should be encased in insulation. Urethane foam used for housing insulation is excellent for this purpose.

Gain is trimmed using the 2kΩ potentiometer. The zero-crossing point is adjusted by changing the value of R_{REF}. Input scaling may be changed by varying resistor R_{IN}.

FIGURE 12: Logarithmic Amplifier with Heated Logging Transistors